LOW POWER HIGH PERFORMANCES ANALYSIS OF IMPACT IONIZATION MOSFET (IMOS) DEVICE

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ABSTRACT. Semiconductor industry is facing several problems in developing silicon devices beyond sub- 100nm such as subthreshold slope swing, increased leakage current leading to high power consumption and heating. Impact Ionization Metal Oxide Silicon Field Effect Transistor (IMOS) is simulated in this paper to investigate the subthreshold slope and leakage current in order to produce high performance transistor in nano scale devices. The electrical characteristics of IMOS are analyzed using the Technology Computer Aided Design (TCAD) simulation. Breakdown characteristics ($I_d – V_s$) and transfer characteristics of IMOS structure are simulated. IMOS operate in lower power consumption due to small leakage current in the device and it only required approximate 3 mV/ decade subthreshold slope to increase the switching speed of the device in MOS technology.

KEYWORDS: Subthreshold Slope, Impact Ionization MOS (IMOS), leakage current

INTRODUCTION

Impact Ionization Metal Oxide Semiconductor (IMOS) was first introduced by Gopalakrishnan et al. in 2002 (Gopalakrishnan et al, 2002). The basic idea of IMOS is based on PiN structure which a gate does not cover entire of the intrinsic area (Choi et al, 2005a; Choi et al, 2005b; Choi, 2009). PiN developed to express the breakdown voltage of IMOS devices as a function of gate and intrinsic lengths and the doping level. At room temperature, subthreshold slope of MOSFET is limited to 60 mV/decade (Khakifirooz and Antoniadis, 2008a; Khakifirooz and Antoniadis, 2008b; Morifuji et al, 2006)). Subthreshold slope of MOSFET determines the ability to turn on and off the device (Moselund et al, 2008). By continued scaling the bias voltage, the subthreshold slope will increase and cause the leakage current increase exponentially and increase the power consumption. IMOS was introduced by Gopalakrishnan et al, 2002. to solve the leakage current and power consumption occurs in MOSFET.

In order to understand and verify the IMOS performances towards low power requirements, the paper is written by comparing the electrical characteristic between nMOS and IMOS using TCAD tools.

DEVICE PHYSICS AND SIMULATION

Figure 1 shows the detailed cross-sections of the device structure which simulated for performance analysis of Lateral Impact Ionization MOSFET using Sentaurus package. This structure comprises of a p+ doped source, a shallow source extension, a drain region with n+
doping, and a lightly doped (n-type) drain extension. The gate is partially covers the intrinsic area. For an n-IMOS, the intrinsic region is p-doped where impact ionization occurs in this region. The electric field required for impact ionization will be reduced in lightly doped region which it can prevent a soft breakdown related to band to band tunneling (Mayer et al, 2006). The lightly doped drain extension reduces the influence of the drain bias on the breakdown voltage and improves the short channel effect control.

Figure 1: Basic Device Structure for N-IMOS

A band gap energy diagram schematic of an n-IMOS in the OFF state and ON state is plotted in the Figure 2. By applying a positive gate voltage to the Gate, the lateral electric field will be increases. The breakdown will be occurs when the critical field is achieved. When apply the gate voltage greater than threshold voltage, it will increase the carrier’s energy. When the energy was increased, it will impact with an atom of the lattice and cause the energy loosed is used to create an electron or hole pair. Avalanche will be breakdown when each carrier produces another pair and so on (Mayer, 2007). These operation reflect the advantages of IMOS device in which the avalanche breakdown was transform into a new paradigm of devices improved.

Figure 2: Band Gap Energy Diagram of n-IMOS
The source was p-doped with Boron with a doping concentration of 1.5x10^{20}/cm^3. The Drain was n-doped with Arsenic with a doping concentration of 9.7x10^{19}/cm^3. The high doped S/D doping was chosen as the device concept was based on impact ionization. IMOS is an impact ionization device with drift current mechanism, which requires high electric fields. Both the drift current and the electric fields depend on the doping concentrations. Hence, high doping concentrations are imperative for obtaining better device characteristics.

The electrical characteristics of devices were done by the solving Poisson’s equation and continuity equation numerically and self-consistently within explicitly defined meshes of the devices (Divya Ravindra and Ismail Saad, 2011). The electrical potential energy and electronic band structures can be computed using Poisson’s equation. Continuity equations for electrons and holes are then used to calculate the current densities of electrons and holes. Boltzmann transport framework is used in solving these two equations. The drift-diffusion transport model with the Boltzmann carrier transport framework was used, as it is able to predict I–V characteristics of IMOS (Jurczak et al, 2001). The Philips unified mobility model is used and high-field saturation effects are accounted for the IMOS. The mobility degradation at the silicon–oxide interface is also accounted for by activating the calculation of the electric field perpendicular to the silicon–oxide interface.

The bandgap narrowing model, the Auger generation–recombination model, and the doping-dependent Shockley–Read–Hall model are activated. The avalanche generation–recombination and band-to-band tunneling models are activated since both these mechanisms contribute to the drain current of the n-IMOS. The contribution of the tunneling mechanism to the drain current is a parasitic effect and degrades the n-IMOS performance. It must be minimized by the proper design of the n-IMOS structure.

**RESULTS AND DISCUSSION**

Figure 3 shows the doping concentration in the drain, source and the intrinsic regions respectively. The boron doping at the source region was shown as 1.5x10^{20}/cm^3, the Arsenic doping at the drain side is 9.7x10^{19}/cm^3, and the intrinsic Silicon layer doping is approximately 1.0x10^{15}/cm^3.
Figure 3: SIMS Profile showing the doping concentration in different regions of nIMOS structure.
Figure 4: Breakdown Characteristic for n-channel IMOS

Figure 4 shows the breakdown characteristic of n-channel IMOS. The breakdown voltage can be defined as the maximum voltage can be applied to a contact. As a result of applying a gate or drain bias of 1V, the breakdown voltage of the n-IMOS is approximate -7.7V. Meanwhile, the device will be cut off when the supply voltage larger than -7.7V and it will be turn on when the supply voltage smaller than -7.7V.

Basically, the IMOS is combination of a p – i – n diode and a MOS transistor (Gopalakrishnan et al, 2005). The transfer characteristic is examined by biasing the drain voltage, $V_D$ and ramping the gate voltage, $V_G$ at defined bias steps. Figure 5 shows the comparison of $I_D - V_G$ characteristics between n-IMOS and n-MOS. From the Figure 5, the simulation was shown the nMOS subthreshold slope is very small compare with the nMOS. Subthreshold slope of the MOS is to determine the ability of the device to turn on or off.
Subthreshold slope of IMOS is much smaller than MOS. It means IMOS is able to turn on device in shorter time compared with MOS due to subthreshold slope of the characteristic. There is no latch up for the IMOS when the gate is switch off due to p-i-n diode in the MOS. This is due to electric fields was reduced less than the breakdown value and the carriers are removed by the drift. As shown in Figure 5 also, IMOS required ‘On’ state current is smaller than MOS which only required 1.23x10^{-4} A compared to 6.435x10^{-4} A. However for the ‘Off’ state current, IMOS required 5.35x10^{-10} A to off the device compared to MOS 1.151x10^{-7} A.

Gate voltage lowers effective the intrinsic silicon length. The lateral Electric field strength increases and causes impact ionization. There are two ways of reduce the breakdown voltage of the IMOS which are intrinsic area can be reduce and introduce a small band gap material (Charbuillet et al., 2006; Onal, 2009). The advantage of IMOS is can produce the low subthreshold swing which approximately 10 mV/decade. However, it have few disadvantages which are the hot electrons of the MOS can destroy the gate oxide and it required a high drain voltage during operation (Savio, 2009).

CONCLUSION

IMOS device operation analyzed toward performances compare to MOS. IMOS is a high speed semiconductor device compare to MOS which it has a very low subthreshold slope approximate 3mV/decade in order to switching the device faster. It also gives better on and off current ratio which achieve low power requirement and high performance for the device. IMOS has the potential replace CMOS in any digital applications due to low power requirement.

However, it found out some of the problems in lateral IMOS. For lateral IMOS, it required high drain voltage to operate it. When the IMOS operate in high temperature, gate oxide of the MOS will be destroying by the electron. To prevent the problem occurs, vertical IMOS can be used.

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REFERENCES


